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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,241	01/30/2004	Mikhail A. Wolf	X-1334 US	8159

24309 7590 09/08/2006

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EXAMINER	
GUTIERREZ, ANTHONY	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 09/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,241	WOLF, MIKHAIL A.	
	Examiner	Art Unit	
	Anthony Gutierrez	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 15-22* is/are pending in the application.

4a) Of the above claim(s) *21 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-12 and 15-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The claims recite generating a new current set of vectors without input of any boundary scan description. The Examiner does not find support for these limitations in the original disclosure.

Applicant's Specification paragraphs 0020 and 0021 address determining initial current test vectors from architecture characteristics, but then the test program generator identifies characteristics of the particular design and boundary scan cells thereof as a function of result data generated by the simulator in response to the test vectors. When test vectors selected for generating a reaction from a particular type of circuit element result in an expected response, the circuit element is mapped to an appropriate boundary scan cell or a pin. The identified characteristics are **used to generate new test vectors.** The Examiner finds all other such support for generating a **new** current set of vectors to be consistent with this example. While this step does not

necessarily rely on a Boundary Scan Description Language (BSDL) file, it does apparently rely on a boundary scan description.

Furthermore, although the generation of the **initial** test vectors is described as occurring from the architecture characteristics, and Applicant's original disclosure is silent about relying or not relying on a boundary scan description for the initial set of vectors, the absence of such disclosure would indicate that generation of the initial set of current vectors is only supported without use of a boundary scan description in as much as that would have been obvious to one of ordinary skill in the art at the time of invention in view of the original disclosure. In other words, the Examiner is not asserting with respect to the **initial** set of current vectors that the limitation regarding without input of any boundary scan description is unsupported, but rather, in order for it to be fully supported, one of ordinary skill in the art at the time of invention would have to conclude from Applicant's original description **alone** that no boundary scan description is used to generated the initial set of vectors. The original disclosure does not seem to teach away from the possibility that a boundary scan description might obviously have been relied on for the initial test vectors from the netlist or architecture characteristics. The Examiner maintains that support regarding the initial set of vectors without input of a boundary scan description, is only found if one of ordinary skill in the art at the time of invention would have concluded such based on a reading of Applicant's description alone because ***if it is considered to be the inventive aspect which overcomes the prior art***, then it should have been **specifically** described that no boundary scan description is relied on (as all known methods would then have relied on a boundary scan description for the initial set of vectors).

Notwithstanding this issue regarding the **initial** set of current vectors, this rejection is specifically made regarding the generation of the **new** set of current vectors as previously addressed.

3. Claims 1-12 and 15-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The claims recite generating a new current set of vectors without input of <u>any boundary scan description</u>. The Examiner does not find support for these limitations in the original disclosure. Therefore, the Examiner does not find a description in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-12, and 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Bruce, Jr. et al. (US Patent 5, 517, 637).

As to claims 1, 10, 11, 15-18, and 20, Bruce, Jr. et al., discloses a computer-implemented method and system for generating a test program for an integrated circuit design employing a boundary scan implementation, including a BSDL file generator, and including a plurality of boundary scan cells coupled to I/0 ports (Title, Abstract, and col. 1, lines 11-50), the method comprising: determining, from a netlist that describes the integrated circuit design, design information including the design architecture and type, name and direction of input and output ports used by the design (col. 3, lines 21-40); generating a current set of verilog test vectors from the design information; simulating the operation of the design using the current set of test vectors and storing result data output during the simulation; generating a new current set of test vectors as a function of the result data; repeating the steps of simulating, storing result data and generating a new current set of test vectors until selected completion criteria are satisfied; and in response to the selected completion criteria being satisfied, generating the test program from the result data (col. 4, lines 30-67 and Figs. 1-3 and col. 6, lines 9-20).

As to the recent amendment of claims 1,15, and 20, that involves limitation involving performing specific steps without input of the boundary scan description of the boundary scan implementation and in response to selected completion criteria being satisfied, generating the boundary scan description from the result data and determining the boundary scan implementation from the result data, the Examiner interprets the reference as follows:

The preamble of the claim provides an antecedent basis for generating a boundary scan description for an integrated circuit design employing a boundary scan implementation.

The Examiner considers the boundary scan *implementation* to be the production test vectors mentioned in col. 6, lines 15-20. These production vectors (this implementation) is based on the boundary scan description that occurs when testing is successful (completion criteria). This is indicated in Fig. 3, box 318.

Successful testing is defined as when no design or definition errors are identified (col. 6, lines 9-14). This is further indicated in Fig. 2, box 212, where detected design and definition errors results in correction of boundary scan descriptions and topology information, and a repetition of certain steps, until no errors are monitored.

The Examiner considers the reference to perform the steps of the claims iteratively until no errors are detected. Although the reference relies on **a** boundary scan description in execution of these steps, it does not (so long as errors are still being identified) rely on **the** (specific) boundary scan description that is ultimately generated on the iteration in which no errors are identified, in which testing is considered successful and from which production vectors are produced. This is what the Examiner considers to be "**the** boundary scan description **of the** boundary scan implementation". Since this particular description is not arrived at until the end of testing, the reference performs the steps iteratively using a boundary scan description, but not **the** description that coincides with "the boundary scan implementation", in other words, it uses a boundary scan description that is not yet completely corrected.

The Examiner therefore considers these limitations to be met by the disclosure of the reference.

Furthermore with respect to claim 20 specifically, the reference teaches that it does not necessarily require **input** of a BSDL file (col. 3, lines 51-55), where Bruce, Jr et al. teaches that the BSDL file can be a pre-existing BSDL file or one generated with the BSDL generation interface. The Examiner maintains that this applies as well for the new comprehensive test vectors. Therefore the rejection is made regarding the reference that relies on a BSDL file but does not necessarily rely on **inputting** the file and therefore anticipates the invention as claimed.

As to claims 2 and 8, Bruce, Jr. et al., discloses storing and using result data indicative of characteristics of design (col. 5, lines 56-65).

As to claim 3, Bruce, Jr. et al., discloses using the stored result data to determine circuit connectivity (col. 5, lines 42-55).

As to claims 4-7, and 9, Bruce, Jr. et al., discloses using the stored result data to map input and output boundary cells to boundary scan access ports (col. 1, lines18-50, and col. 3, line 41-col. 4, line 16, with respect to the discussion of the boundary scan register as it relates to the input/output, access ports, and cells).

As to claim 12, Bruce, Jr. et al., discloses generating new test vectors that use the identified circuit characteristics (See Fig. 2, boxes 208 and 216).

As to claim 19, Bruce, Jr. et al., discloses that the integrated circuit design includes at least two distinct circuits, each distinct circuit having test I/O ports and associated boundary scan cells coupled thereto, the plurality of boundary scan cells being coupled in a chain with output boundary scan cells from a first one of the at least

two distinct circuits being coupled to input boundary scan cells of a second one of the at least two distinct circuits, wherein the storage circuit is adapted to store result data indicative of the chain connectivity of the output boundary scan cells to the input boundary scan cells and wherein the test program generator is adapted to generate the boundary scan description as a function of the chain connectivity (col. 1, lines 18-31)

Response to Arguments

6. Applicant's arguments filed 2/17/06 have been fully considered but they are not persuasive.

Applicant has amended claims 1-12 and 15-19 in a way that does not appear to be fully supported by Applicant's original disclosure. Although the Amendments appear to overcome the reference with respect to the limitations in the claims, the Examiner has presently included new grounds of rejection under 35 U.S.C. 112 first paragraph regarding these limitations. The Examiner therefore maintains his previous prior art rejection under 35 U.S.C 102 regarding these claims and is not persuaded that Applicant's amendment has resulted in proper claims that overcome the prior art of record.

The Examiner has slightly modified his rejection of claim 20 to address Applicants amendment of the claim.

The Examiner previously restricted claims 21 and 22 by original presentation from the pending claims. The Examiner is not persuaded by Applicant's arguments that the claims should be reinstated due to their similarity to claim 21(which the Examiner

presumes was intended by Applicant to be claim 1) because the broad and specific nature of the subcombination not essential to the combination (addressed in the previous Office Action) is found only in the limitations of claims 21 and 22 and not the other claims as provided previously or as amended.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

United States Patents

U.S. Patent No. 7,073,111 B2 to Whetsel teaches a high speed interconnect circuit test method including JTAG boundary scan cells.

U.S. Patent No. 6,988,229 B1 to Folea, Jr., teaches a method for monitoring and controlling boundary scan enabled devices that does not require the use of test vectors.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Gutierrez whose telephone number is (571) 272-2215. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on (571) 272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AG
Anthony Gutierrez

9/1/06

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